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Low-Voltage Bendable Pentacene Thin-Film Transistor with Stainless Steel Substrate and Polystyrene-Coated Hafnium Silicate Dielectric

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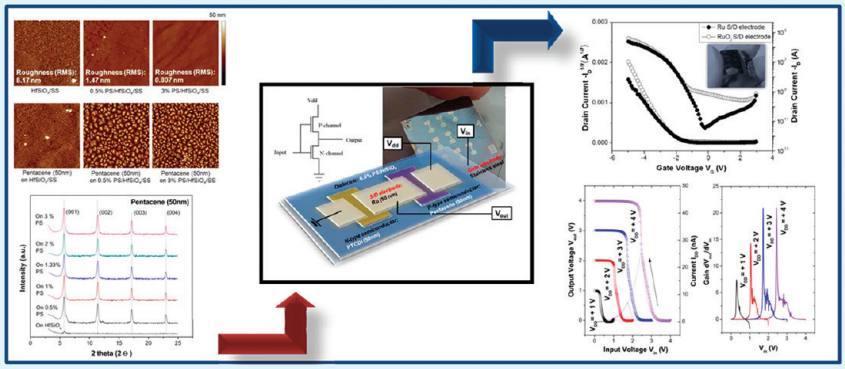

ABSTRACT: The hafnium silicate and aluminum oxide high-k dielectrics were deposited on stainless steel substrate using atomic layer deposition process and octadecyltrichlorosilane (OTS) and polystyrene (PS) were treated improve crystallinity of pentacene grown on them. Besides, the effects of the pentacene deposition condition on the morphologies, crystallinities and electrical properties of pentacene were characterized. Therefore, the surface treatment condition on dielectric and pentacene deposition conditions were optimized. The pentacene grown on polystyrene coated high-k dielectric at low deposition rate and temperature (0.2−0.3 Å/s and R.T.) showed the largest grain size (0.8−1.0 μm) and highest crystallinity among pentacenes deposited various deposition conditions, and the pentacene TFT with polystyrene coated high-k dielectric showed excellent device-performance. To decrease threshold voltage of pentacene TFT, the polystyrene-thickness on high-k dielectric was controlled using different concentration of polystyrene solution. As the polystyrene-thickness on hafnium silicate decreases, the dielectric constant of polystyrene/hafnium silicate increases, while the crystallinity of pentacene grown on polystyrene/hafnium silicate did not change. Using low-thickness polystyrene coated hafnium silicate dielectric, the high-performance and low voltage operating (<5 V) pentacene thin film transistor (μ: ~2 cm^2/(V s), on/off ratio, >1 × 10^4) and complementary inverter (DC gains, ~20) could be fabricated.

KEYWORDS: *polystyrene, octadecyltrichlorosilane, ruthenium, atomic layer chemical vapor deposition, hafnium silicate, pentacene thin film transistor*

1. INTRODUCTION

To fabricate high-performance organic thin film transistors (OTFT), research effort has been focused on improving the electrical properties of the semiconductor as well as the gate dielectric and conducting electrodes.[1−4] The mobility and on/off ratio of organic TFT with pentacene have been continuously improved[1−4] but the performance of OTFTs is still poor compared to that of the conventional inorganic TFTs, because of the difficulties in optimizing each device component such as crystallinity of organic semiconductor, device architecture, and interfaces. A great deal of studies have been required on various systems such as modification of organic semiconductor or dielectric layer, substitution of the electrode materials, insertion of additional layers in organic semiconductor/dielectric, or electrode/organic semiconductor interface.[1,5−8]

To control the charge carrier in the channel region of organic semiconductor more efficiently, researchers have studied various high-k materials, such as Al_2O_3, Ta_2O_3, TiO_2, BST, and HfO_2, for the substitution of a dielectric layer as well.[9−14] Among those high-k materials, hafnium silicate ($HfSiO_x$) and aluminum oxide (Al_2O_3) were recently studied by our group to evaluate performances of them as gate dielectrics of pentacene TFTs.[15,16] Actually, both pentacene TFTs with Al_2O_3 and $HfSiO_x$ gate dielectrics showed high performance but the pentacene TFT with $HfSiO_x$ gate dielectric shows higher mobility and low threshold voltage than that with Al_2O_3 gate dielectric owing to high-k dielectric constant value (Al_2O_3,~9; $HfSiO_x$, ~11).[15]

On the other hand, the crystallinity or orientation of organic semiconductor is one of the critical factors determining

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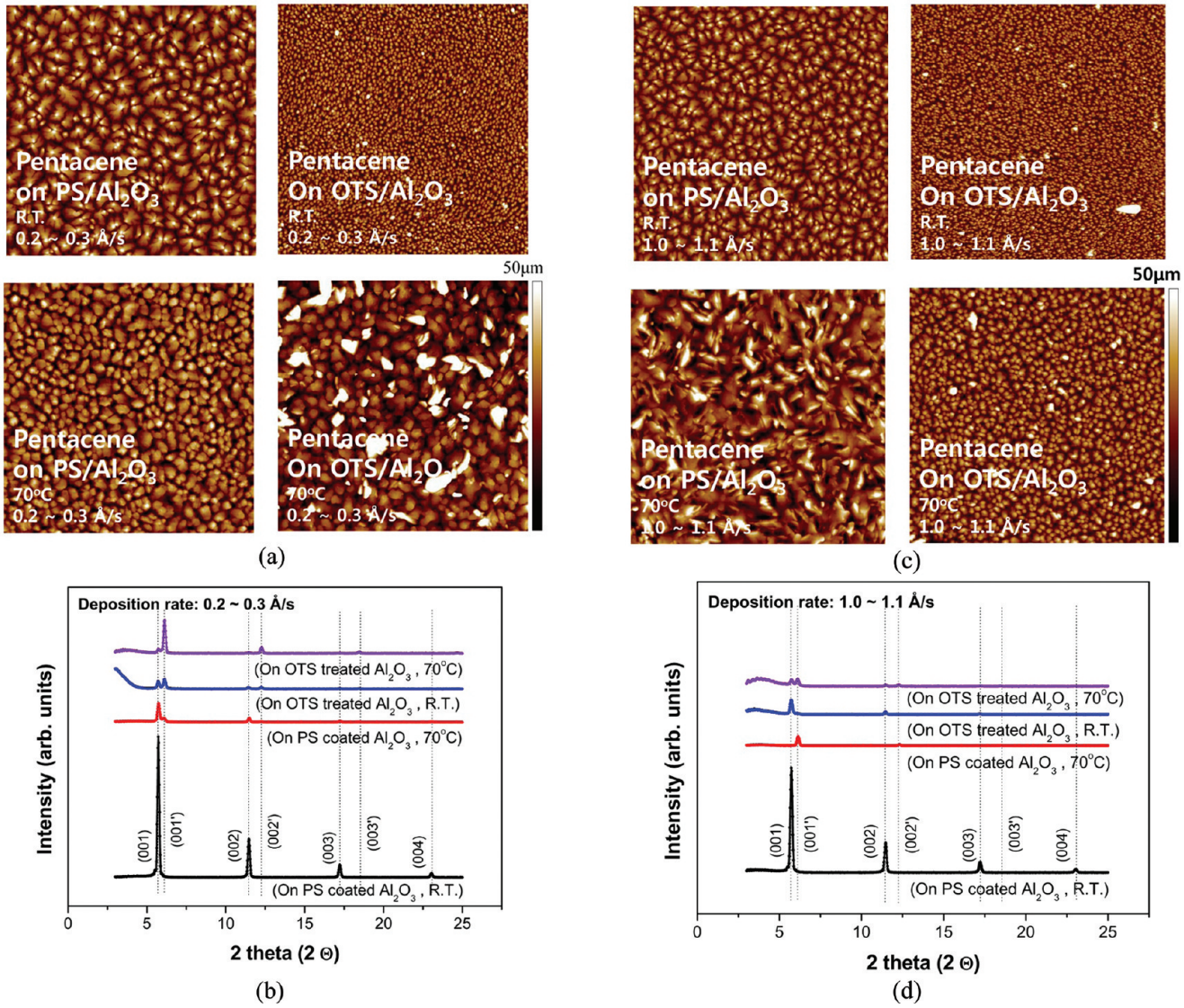

Figure 1. AFM images (10 μm × 10 μm, (a) 0.2−0.3 Å/s and (c) 1.0−1.1 Å/s) and XRD spectrum ((b) 0.2−0.3 Å/s and (d) 1.0−1.1 Å/s) of of the pentacene layer (50 μm) grown on the OTS-treated and PS-coated Al_2O_3/SS at different deposition rate and temperature conditions.

mobility, on/off ratio and threshold voltage of the device, and it is highly dependent on the various deposition conditions (roughness and surface energy of the substrate and buffer layer, and the deposition temperature and deposition rate). For this reason, a great number of studies, which analyzed the relationship between deposition condition and the properties of organic semiconductor (or the performance of OTFT), have been actively reported for decades.[9,18−24] The organic semiconductor grown on inorganic dielectric is not well oriented or well crystallized because of the low surface energy and high roughness. Therefore, it was expected that the surface treatments such as polystyrene (PS) coating and octadecyltrichlorosilane (OTS) treatment, which are widely utilized for improving the crystallinity, carrier mobility, and orientation of pentacene grown on gate dielectric layer,[5,18−22] would improve the properties of organic semiconductor grown on the high-k gate dielectrics ($HfSiO_x$ and Al_2O_3). The effect of PS coating or OTS treatment on the orientation and electrical properties of pentacene layer was studied, but there are not many reports that directly compare and analyze the influence on the properties of pentacene layer and the electrical properties of the devices.

Additionally, stainless steel (SS), which has high thermal and chemical stability, high electrical conductivity, and bendable properties, was applied to gate electrode as well as substrate.[15−18] The high surface roughness, which is the main drawback of SS substrate to be applied to organic device, was solved by the chemical mechanical polishing (CMP) polishing process using optimized conditions.[15,18]

In this work, the effects of surface treatment (OTS treatment and PS coating on high-k dielectric layer) and deposition condition (deposition rate and temperature of pentacene) on the performance of pentacene TFTs were clearly compared and analyzed. On the basis of this study, the fabrication process of pentacene TFT with high-k dielectric was optimized and low operating voltage pentacene TFT and complementary inverter with PS/$HfSiO_x$ dielectric layers were fabricated on SS.

2. EXPERIMENTAL SECTION

The 304 SS substrates (surface roughness, ~35 nm) supplied by POSCO were polished with CMP process (KEMET P25FRS-A3) with

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alumina slurry of 0.05 μm diameter for 20 min; they were then washed with distilled water and acetone.

$HfSiO_x$ dielectric layer was deposited on SS substrate by an atomic layer deposition (ALD) process. Precursor combination of $Hf(N(CH_3)(C_2H_5))_4$ (TEMAH) and $Si(OC(CH_3)_3)_4$ (TBOS) were used without additive oxidant. The temperature of TEMAH and TBOS bubbler were fixed at 70 and 85 °C, respectively, and the temperature of transport lines were maintained at 95 °C to avoid any condensation of precursors. Argon (99.9995%) was used as a buffer flow to keep an overall flow uniform and also a carrier gas to transport precursor vapors into the chamber. The flow rate of the Ar carrier gas and buffer gas were fixed at 25 and 300 sccm, respectively. The films were deposited at a growth temperature of 300 °C and a pressure of 0.80 Torr. The ALD cycle was TEMAH injection (7 s)−purge (7 s)−TBOS injection (10 s)−purge (7 s). The detailed of deposition process is reported elsewhere.[18]

In the deposition process of Al_2O_3 dielectric layer, trimethyl aluminum and distilled water were employed as a precursor and an oxidizing reaction gas. The line from the precursor bottle to the reactor was maintained at 60 °C and the pressure and temperature of the reactor were fixed at 1 Torr and 150 °C, respectively. N_2 (99.999%) gas was employed as a carrier and purge gas. Flow rate of N_2 gas for purging and carrying vaporized water was fixed at 100 and 10 sccm, respectively. The ALD cycle of Al_2O_3 film was precursor injection (1 s)−purge (5 s)−water vapor injection (1 s)−purge (10 s).[15]

For OTS treatment on Al_2O_3 dielectric layer, the substrate was dipped in the 1 mM OTS-toluene (purchased from Aldrich Chemical Co.) solution for 2 h at a low temperature of ∼4 °C and washed out in toluene and acetone for 30 min each with sonication. Finally, OTS-treated substrate was annealed in a vacuum chamber for 2 h at 120 °C and kept in vacuum chamber at 50 °C. Various concentrations of PS solutions (0.5, 1, 1.33, 2, and 3% in toluene) were employed and spin-coated at 5000 rpm for 30 s. The MIM structures of Au/PS/$HfSiO_x$/SS were fabricated using different concentration of PS solutions and the leakage currents and dielectric constants of them were characterized.

Pentacene thin films of 50 nm thickness were deposited on OTS treated Al_2O_3 (OTS/Al_2O_3), PS-coated Al_2O_3 gate dielectric (PS/Al_2O_3) and PS-coated $HfSiO_x$ gate dielectric (PS/$HfSiO_x$) at R.T. and 70 °C using an organic molecular beam deposition (OMBD) system at 2×10^{-6} Torr. As a S/D electrode, Au and Ru (and RuO_2) were deposited using a thermal evaporator and radio frequency magnetron sputtering, respectively. And the S/D electrodes were patterned using shadow mask during deposition process (channel length, 150 μm; width, 1500 μm). To prevent the penetration of S/D electrode into the channel region, substrate was tightly fixed between shadow mask and magnet support. Besides, the complementary inverter was also fabricated using optimized preparation condition of PS/$HfSiO_x$ dielectric. The same procedures were used to fabricate an inverter (channel length: 100 μm and channel width: 1000 μm). N,N′-Ditridecyl-3,4,9,10-perylenetetracarboxylic diimide (PTCDI-C13) film, which is most widely used n-type semiconductor because of high mobility, was deposited at room temperature with a rate of 0.2−0.3 Å/s in an OMBD system.

The phases and crystallinities of pentacene grown on different substrates at different temperature were examined by X-ray diffraction (XRD) with 3C2 beamline at the Pohang Accelerator Laboratory. The morphology and surface roughness of pentacene and high-k dielectric on SS were investigated with atomic force microscope (AFM in NCNT). The thicknesses of dielectrics layers and the contact angles of PS/$HfSiO_x$ were measured using ellipsometry and D.I. water sessile drop method, respectively. The capacitance−voltage (C−V) measurements were performed at at a high frequency (1 MHz) using a HP 4275 multifrequency LCR meter. The current−voltage (I−V) characteristics of the MIM structure and pentacene TFTs were measured at room temperature using Agilent E5270A precision semiconductor parameter analyzer.

3. RESULTS AND DISCUSSION

Figure 1 shows AFM images (10 μm × 10 μm, (a): 0.2−0.3 Å/s and (c) 1.0−1.1 Å/s) and XRD spectrum (b): 0.2−0.3 Å/s and (d) 1.0−1.1 Å/s) of the pentacene layer (50 μm) grown on OTS/Al_2O_3 and PS/Al_2O_3 at different deposition rate and temperature conditions. Grain size and crystallinity of pentacene highly depend on the roughness and surface energy of substrate. The pentacene grown on Al_2O_3/SS substrate at R.T. showed small grain size and poor crystallinity due to hydrophilic (high surface energy) property and high roughness of Al_2O_3/SS substrate.[18−25] Both PS coating and OTS treatment on Al_2O_3/SS substrate reduced surface energy (contact angle of D.I. water, ∼90° on PS-coated and ∼107° on OTS-treated Al_2O_3/SS) and especially, PS coating showed an significant effect on reducing surface roughness as well as surface energy.[18,22,23,25,26] As a result, the pentacene grown on PS/Al_2O_3 at R.T. (of deposition rate: 0.2−0.3 Å/s) showed typical terrace-like structure with large grain size (0.8−1.0 μm) but the pentacene grown on OTS/Al_2O_3 consists of round-shape structure with small grin size (0.05−0.1 μm) due to high roughness, in spite of low surface energy, as compared in Figure 1a.[18,22,23,26]

On the other hand, the properties of pentacene grown at 70 °C differ from those of pentacene grown at R.T., because the glass transition temperature (T_g) of PS thin film is almost closed to 70 °C and pentacene diffuses well at high temperature.[9,22,24,25] Therefore, at the deposition temperature of 70 °C, the grain size of pentacene grown on PS/Al_2O_3 decreases (0.3−0.5 μm) and the pentacene on OTS/Al_2O_3 forms larger grain size (0.5−0.7 μm) compared to that grown at R.T., respectively. In case of pentacene thin layer (∼50 nm) on PS/Al_2O_3 and OTS/Al_2O_3, the thin-film phase (001 at 5.74°, 15.4 Å) and bulk pentacene phase (001′ at 6.15°, 14.5 Å) predominates at low deposition temperature (R.T.) and at high deposition temperature (70 °C), respectively.[20−25] And the crystallinities of pentacene layers on PS/Al_2O_3 on OTS/Al_2O_3 were closely correlated with the grain size of them, as shown in Figure 1a−d.[20−25] The pentacene (∼50 nm) grown on PS/Al_2O_3 at R.T. shows the highest diffraction intensity of thin film phase than those grown at other conditions, but the diffraction intensity of thin film phase was decreased and bulk pentacene phase appeared as the deposition temperature increases.[24] Besides, the pentacene consisting of small grain grown on OTS/Al_2O_3 at R.T. showed poor crystallinity of the thin film phase and bulk pentacene phase mixture but the pentacene consisting of large grain grown on OTS/Al_2O_3 at 70 °C shows the high crystallinity of bulk pentacene phase.[25−29]

Because of the high mobility of pentacene molecule, the pentacene layer grown on OTS/Al_2O_3 at 70 °C formed larger grain than that grown at low temperature. But the pentacene layer on PS/Al_2O_3 showed different behavior due to low T_g. The morphology change of PS near T_g interrupted the formation of large grain during pentacene deposition at 70 °C

The deposition rate of pentacene also has an effect on the crystallinity and morphology of pentacene.[20,24,25] All other conditions being equal (deposition temperature or substrate), comparing pentacene deposited at 0.2−0.3 Å/s with that deposited at 1.0−1.1 Å/s, the pentacene deposited at 0.2−0.3 Å/s shows higher crystallinity and larger grain size, as summarized in Figure 1a−d.

To compare the electrical properties of pentacene grown on OTS/PS to those of pentacene grown on OTS/Al_2O_3, the

OTFTs with pentacene grown on OTS/Al_2O_3 at 70 °C and PS (2%)/Al_2O_3 at R.T. were fabricated and performance of them were compared as shown in Figure 2a, b. Figure 2a shows the

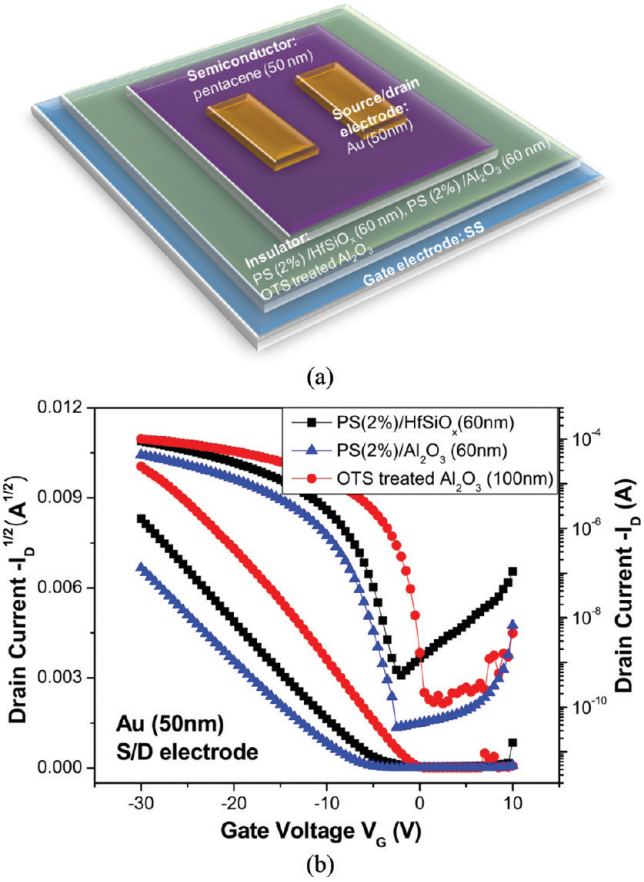

Figure 2. (a) Schematic structure and (b) comparative transfer characteristics of the top contact pentacene TFTs with OTS-treated, PS (2%)-coated Al_2O_3/SS, and PS (2%)-coated $HfSiO_x$/SS.

schematic structure of pentacene TFTs with pentacene grown on OTS/Al_2O_3 and PS (2%)/Al_2O_3. The field-effect mobility in the saturated regime (V_D = −40 V) was calculated using the formula given below[1]

$$I_{DS} = \frac{WC_i}{2L}(V_G - V_T)^2\mu \quad (1)$$

where I_{DS} is the drain current at specific gate voltage (V_G), W is the channel width, L is the channel length, V_T is the threshold voltage, μ is the carrier field effect mobility and C_i is the capacitance per unit area of the gate insulator. The OTS treatment on Al_2O_3 dielectric layer removes trap and scattering site near the channel region and improves the orientation of pentacene molecule grown on dielectric layer. The pentacene TFT with OTS/Al_2O_3 showed the excellent electrical properties including high saturation on-current, low threshold voltage and low subthreshold swing.[15] In spite of the high dielectric constant of OTS/Al_2O_3, the actual field-effect mobility (at V_D = −40 V) of pentacene TFT with PS (2%)/Al_2O_3 was much higher (1.31 cm^2/(V s)) than that with OTS/Al_2O_3 (0.496 cm^2/(V s)) owing to high crystallinity of pentacene semiconductor.[30] As a result, it is believed that the PS coating is more efficient way to improve not only the properties of pentacene but also the electrical properties of pentacene TFT compared with OTS treatment.

On the other hand, the pentacene TFT with PS (2%)/Al_2O_3 has too high threshold voltage to be employed in low-voltage operation in spite of high field-effect mobility. To reduce the threshold voltage further, the Al_2O_3 dielectric was replaced with the $HfSiO_x$ dielectric, which has a higher dielectric constant than that of Al_2O_3, because the electric carrier near channel region of organic semiconductor would be controlled more promptly by gate dielectric of higher dielectric constant.[18,31−33] Actually, the pentacene TFT with PS (2%)/$HfSiO_x$ showed slightly higher field-effect mobility of 1.48 cm^2/(V s) and lower threshold voltage of −5.49 V than that with PS (2%)/Al_2O_3 (μ, 1.31 cm^2/(V s)l V_T, −7.79 V). Table 1 shows the device characteristics of pentacene TFTs with PS-coated and OTS treated high-k dielectrics (Al_2O_3 and $HfSiO_x$).

Subsequently, the effects of PS-thickness on the properties of PS/$HfSiO_x$ dielectric and pentacene grown on PS/$HfSiO_x$ were studied. As the PS concentration in solution decreases, the PS thickness on $HfSiO_x$ decreased, whereas the hydrophobicity related to surface energy was constantly maintained. As shown in Figure 3a, the contact angles of D.I. water on various concentration of PS coated $HfSiO_x$/SS substrate showed similar contact angle around 90 ± 3 ° regardless of PS-thickness. The leakage currents (A/cm^2) of PS/$HfSiO_x$ were compared using MIM structure of Au/PS/$HfSiO_x$/SS and the current density at the same voltage decreased as increase of PS concentration in solution, as shown in Figure 3b.

On the other hand, the dielectric constant of PS/$HfSiO_x$ bilayer could be calculated by following equation

$$1/C_{PS/HfSiOx} = 1/C_{PS} + 1/C_{HfSiOx} \quad (2)$$

or directly measured using MIM structure of Au/PS/$HfSiO_x$/SS. Actually, the experimental dielectric constants of PS/$HfSiO_x$ dielectrics were almost same with theoretical dielectric constants and the dielectric constants decreased with increase of the thickness of PS on $HfSiO_x$.[32] The dielectric constants of PS (0.5%, 21.2 nm)/$HfSiO_x$ and PS (3.0%, 95.4 nm)/$HfSiO_x$ were measured to 6.11 and 2.55, respectively.

Panels a and b in Figure 4 show the morphologies of various PS/$HfSiO_x$/SS and pentacene grown on them and the XRD patterns of pentacenes grown on various PS/$HfSiO_x$/SS, respectively. The roughness value (rms = 8.17 nm) of $HfSiO_x$/SS significantly decreased after PS coating on it, and the PS (0.5%, 21.2 nm)/$HfSiO_x$/SS showed low roughness value of 1.47 nm, which is comparable to that of PS (3%, 95.4 nm)/$HfSiO_x$/SS (rms = 0.807 nm). As already mentioned, the morphology and crystallinity of pentacene are highly dependent on the roughness of substrate and the pentacene grown on smooth substrate generally shows large grain size and high crystallinity. Although the pentacene grown on rough and hydrophilic $HfSiO_x$/SS form small round grain and low crystallinity, every pentacene grown on PS/$HfSiO_x$/SS formed a pyridine structure with large grain size and high crystallinity, as shown in panels a and b in Figure 4 . Especially, it was confirmed that the pentacene grown on low thickness of PS-coated $HfSiO_x$/SS also shows similar film properties with that grown on high thickness of PS coated $HfSiO_x$/SS.

The top-contact pentacene TFTs with different concentration of PS-coated $HfSiO_x$/SS were fabricated using Ru (or RuO_2) S/D electrode, to analyze the effect of PS layer thickness on threshold voltage of device. The pentacene TFTs with Ru S/D electrode and PS/$HfSiO_x$/SS showed high performance

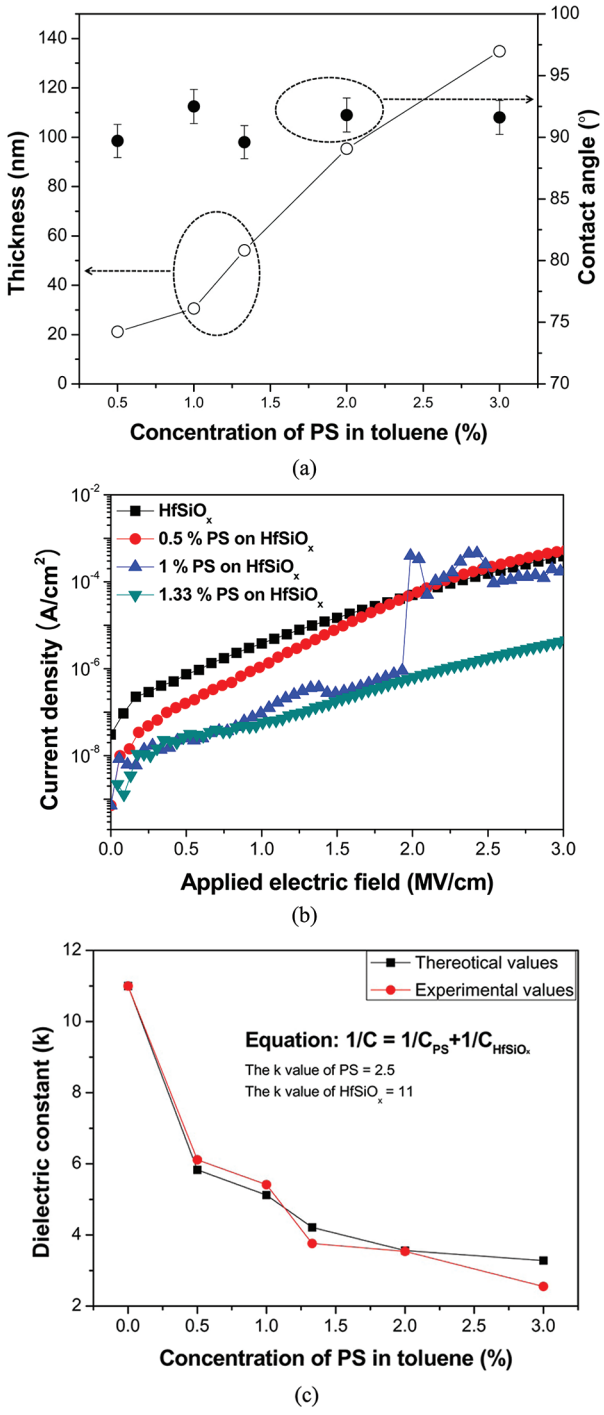

Figure 3. Changes in (a) PS-thickness and contact angle, (b) leakage current, and (c) dielectric constant as a function of the PS concentration in toluene.

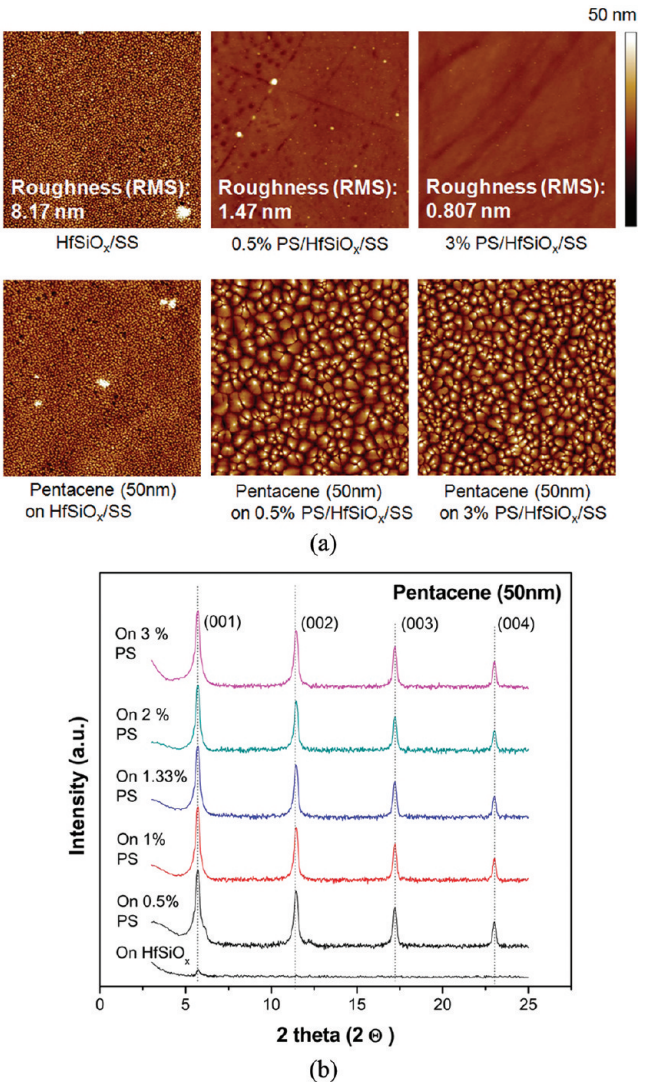

Figure 4. (a) AFM images (10 μm × 10 μm) of different concentration of PS-coated $HfSiO_x$/SS and pentacene layers on them and (b) XRD spectrum of pentacene layers on various concentration of PS-coated $HfSiO_x$/SS.

and their device characteristics were comparable to that with pentacene TFT with Au S/D electrode, as shown in panels a and b in Figure 5. The pentacene TFTs with Ru S/D electrode and PS/$HfSiO_x$/SS showed similar levels of μ (~ 1 $cm^2/(V\,s)$) and on/off ratio (~1 × 10^4), but the threshold voltage of them decreased as a function of PS concentration, as summarized in Table 2 and Figure 6a. Therefore, operating pentacene TFT within low voltage of 5 V became available using low concentration of PS coated $HfSiO_x$ gate dielectric.

Panels b and c in Figure 6 show the comparable transfer curve and output curve of top-contact pentacene TFTs with Ru and RuO_2 S/D electrodes and PS (0.5%, 21.2 nm)/$HfSiO_x$/SS, which were operated within 5 V, respectively. Owing to low threshold voltage of −2.40 V, devices operated well as a transistor within 5 V, as shown in transfer and output characteristics of panels a and b in Figure 6 . Especially, the transfer characteristic of the top contact pentacene TFT with RuO_2 S/D electrode was deteriorated at off current region. We believe that the pentacene layers would be damaged by activated oxygen radical or ions during RuO_2 sputtering deposition process, and this induced the leakage current from source to drain at low gate voltage bias. Nevertheless, the pentacene TFT with RuO_2 S/D electrode showed higher μ over 2 $cm^2/(V\,s)$ than that of Ru S/D electrode (~ 1 $cm^2/(V\,s)$), because the low hole-injection barrier between S/D electrode and pentacene reduces contact resistance.[34]

Figure 7a shows schematic structure of complementary inverter composed of p-type (pentacene) and n-type (PTCDI-C13) TFTs. Complementary inverter is operated by the complementary turning on and off operation of p-type

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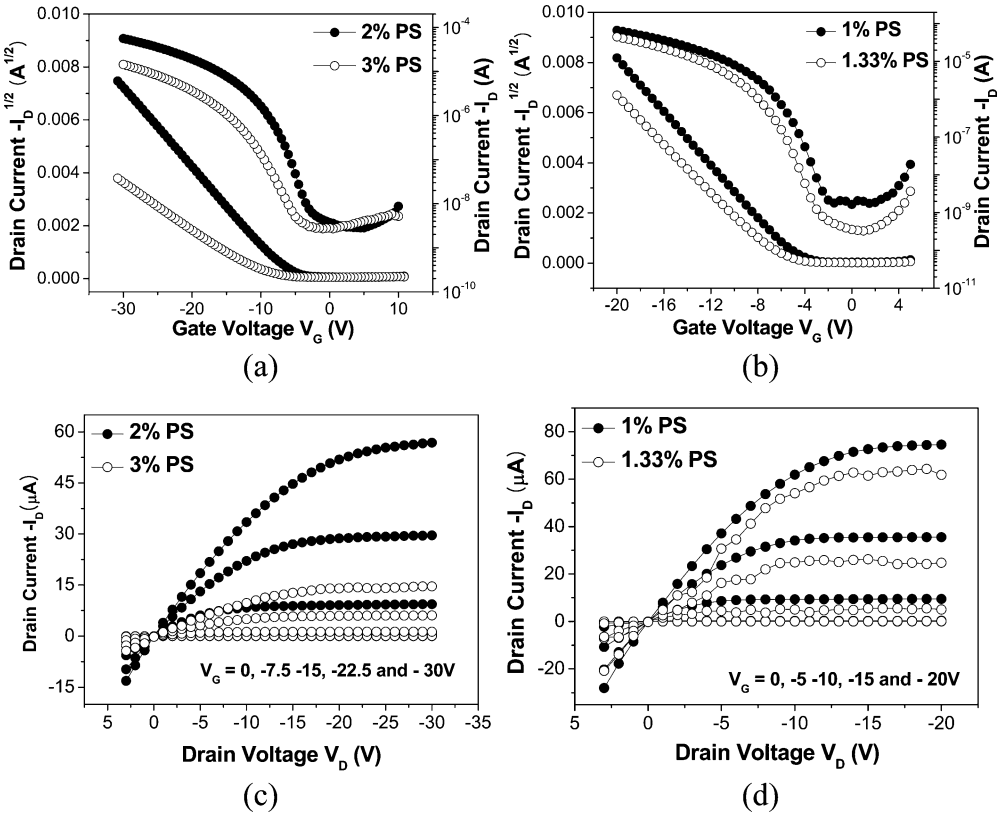

Figure 5. Transfer ((a) 2 and 3% and (b) 1 and 1.33%) and output characteristics ((c) 2 and 3% and (d) 1 and 1.33%) of the pentacene TFT with different concentration of PS-coated $HfSiO_x$/SS and Ru S/D electrode.

Table 1. Device Characteristics of Pentacene TFTs with PS-Coated and OTS-Treated High-k Dielectrics

dielectric	S/D electrode	thickness (nm)	dielectric constants(k)/ capacitance per unit area (nF/cm^2)	operating voltage (V)	field-effect mobility(cm^2/(V s))	on/off current ratio	threshold voltage (V_{th})	sub threshold swing (V/dec)
PS (2%) /$HfSiO_x$	Au (50 nm)	155.4	3.54/16.0	−30	1.48 ± 0.1	2 × 10^5	−5.49	1.31
PS (2%) /Al_2O_3		155.4	2.90/13.1		1.31 ± 0.1	∼1 × 10^5	−7.79	1.36
OTS treated Al_2O_3		∼100	∼9/∼65		0.496 ± 0.05	8 × 10^5	−1.02	0.642

Table 2. Device Characteristics of Pentacene TFTs with Different Concentration of PS-Coated $HfSiO_x$ Dielectrics

dielectric	S/D electrode	thickness (nm)	dielectric constant k/ capacitance per unit area (nF/cm^2)	operating voltage (V)	field-effect mobility (cm^2/(V s))	on/off current ratio	threshold voltageV_T (V)	sub threshold swing (V/dec)
3.0% PS on $HfSiO_x$	Ru	194.8	2.55/10.1	−30	0.70 ± 0.05	∼1 × 10^4	−9.87	3.35
2.0% PS on $HfSiO_x$	Ru	155.4	3.54/16.0		1.24 ± 0.1	∼1 × 10^4	−6.15	2.24
1.33% PS on $HfSiO_x$	Ru	114.2	3.76/33.0	−20	1.32 ± 0.1	∼5 × 10^4	−5.84	1.36
1.0% PS on $HfSiO_x$	Ru	90.6	5.41/45.9		1.24 ± 0.1	∼5 × 10^4	−4.66	1.26
0.5% PS on $HfSiO_x$	Ru	81.2	6.11/57.9	−5	1.07 ± 0.1	∼1 × 10^5	−2.41	0.32
	RuO_2				2.05 ± 0.1	∼1 × 10^4	−2.39	0.65
$HfSiO_x$	Au	60	11	−10	∼0.93 ± 0.1	∼1 × 10^4	−1.02	0.47

(pentacene) and n-type (PTCDI-C13) TFTs and the output voltage (V_{out}) stayed close to supply voltage (V_{DD}) at low input voltage (V_{in}) and abruptly dropped to 0 V above the specific V_{in}.[35,36]

As shown in panels b and c in Figure 7, complementary inverters showed suitable $V_{out} - V_{in}$ characteristics and high DC gains (dV_{out}/dV_{in} = 20), but the falling slope between V_{out} and V_{in} was getting smaller as the V_{out} approaches to 0 V. Complementary inverter is operated by the complementary

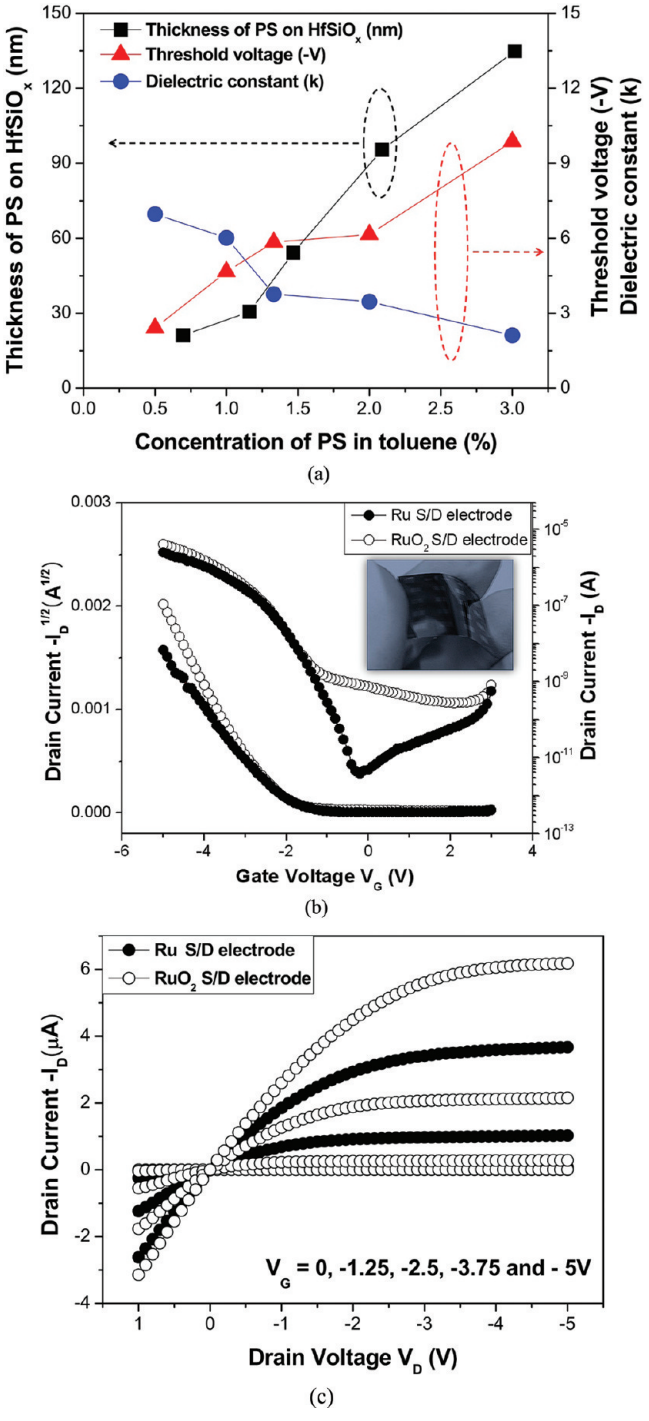

Figure 6. (a) Organized graph indicating the dependence of PS-thickness, dielectric constant of PS/HfSiO$_x$, and threshold voltage of pentacene TFT on concentration of PS in toluene and (b, c) comparative transfer and output characteristics of the pentacene TFTs with Ru and RuO_2 S/D electrode and PS (2%)/HfSiO$_x$/SS.

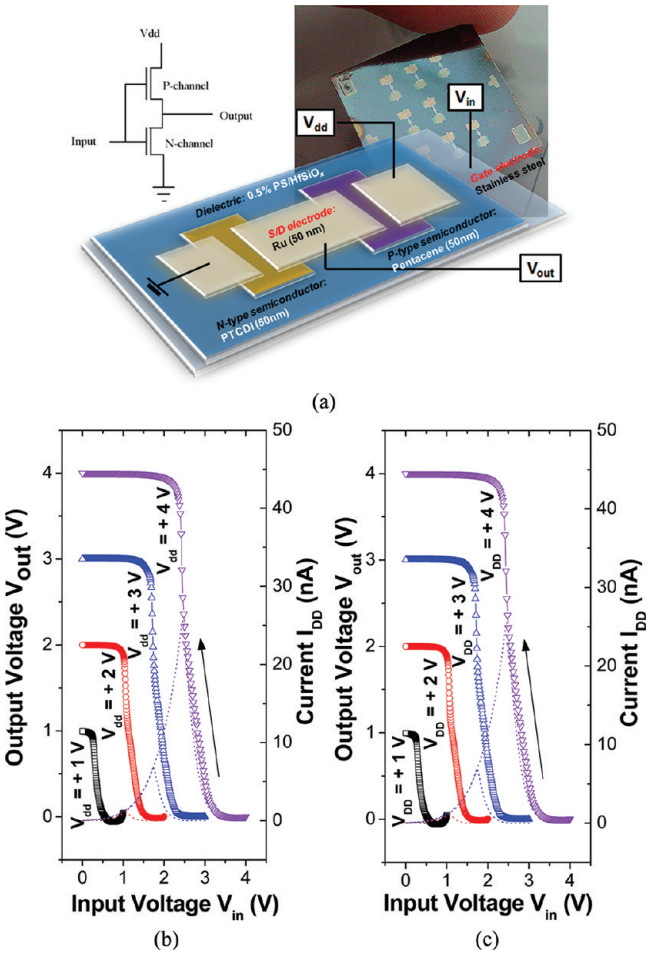

Figure 7. (a) Schematic structure, (b) the voltage transfer characteristics, and (c) DC gain with various V_{DD} values of complementary inverter with PS/HfSiO$_x$ dielectric.

turning on and off operation of p-type (pentacene) and n-type (PTCDI-C13) TFTs and the V_{out} stayed close to V_{DD} at low V_{in} and abruptly dropped to 0 V above the specific V_{in} due to poorer saturation mobility of n-type TFT ($\mu \approx 0.01$ cm^2/(V s) and on/off ratio = 1×10^3) with p-type TFT. Actually, the μ of n-type TFT was near ~0.01 cm^2/(V s), which is almost 100 times lower than that of p-type TFT in the same inverter device, and low mobility of n-type TFT was due to the poor crystallinity of PTCDI-C13 on PS/HfSiO$_x$, as already studied by Jang et al.[36]

4. CONCLUSION

In summary, the pentacene grown on PS-coated substrate at low deposition rate and temperature (0.2−0.3 Å/s and R.T.) showed the largest grain size and highest crystallinity among pentacene layers deposited at various deposition conditions, and the pentacene TFTwith PS treated high-k dielectric shows more excellent device-performance than that with OTS-treated dielectric. Furthermore, to compensate for increase of threshold voltage thatwas induced by the low dielectric constant of PS coating on HfSiO$_x$ dielectric, the PS thickness on HfSiO$_x$ was controlled and the HfSiO$_x$. Both pentacene TFT and complementary inverter with PS (0.5%, 21.2)/HfSiO$_x$/SS and Ru S/D electrode (or RuO_2 S/D electrode) were operated within 5 V, and the electrical performance of them were also excellent.

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Notes

The authors declare no competing financial interest.

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